19.7 A Polar Loop Transmitter with Digital Interface including a Loop-Bandwidth Calibration System

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Low cost, low power consumption, and small size are important features for mobile phone RF solutions. Recently, there has been increasing interest in the integration of RFICs and baseband LSIs (BBLSIs) on the same chip [1]. An integrated solution would be suitable for single function mobile phones. However, many handsets contain not only a mobile phone interface, but also digital TV, GPS, WLAN, and other wireless application interfaces, and each of those applications requires its own BBLSI function. Therefore, it is not very efficient to integrate an RF and several BB sections on a single chip. The digital interface is a new partition between RFICs and BBLSIs for solving the above issues. Digital interface RFICs include ADCs, DACs, and digital filters. They communicate with the BBLSI through digital serial data lines. Therefore, BBLSI can be designed with the most advanced process available without any analog options.

RFIC with digital interface for GSM/EDGE is fabricated in a 0.18μm SOI BiCMOS process. Figure 19.7.1 shows the block diagram of the developed RFIC. It adapts to GSM850, GSM900, DCS1800, and PCS1900 bands. The receiver uses direct-conversion (zero-IF) architecture and includes LNAs, I/Q demodulators, ADCs, and digital filters. The transmitter uses polar loop [2] architecture that operates as offset PLL in GSM mode and polar loop transmitter in EDGE mode. The transmitter receives binary data from BBLSI via a digital interface. The GMSK or 8PSK digital filter is used to generate the GSM or EDGE modulated signal. The modulated signal is upconverted by an I/Q modulator to an intermediate frequency that is around 70 to 100MHz. In the case of GSM, since the modulated signal has constant amplitude, it can only be generated using a phase modulation (PM) loop. In the case of EDGE, an amplitude modulation (AM) loop is additionally applied to add amplitude signal. Both the AM and PM signals are controlled by negative feedback loops and they are robust against AM-AM, and AM-PM distortion.

Variation of the PM loop bandwidth from the designed value degrades the offset noise levels specified by the standard [3]. When the PM loop bandwidth is narrower than the designed bandwidth, the noise level near the center frequency of the modulated signal, such as the 400kHz offset and 600kHz offset, degrades. When the PM loop bandwidth is wider than the designed bandwidth, the noise level of the out of loop bandwidth, such as 1.8MHz and 20MHz, degrades. The variation of the PM loop bandwidth happens because of the sensitivity of the VCO, that changes at every frequency hop, the process variation of capacitances in the integrated loop filter, and the thermal and supply voltage dependencies. To achieve the specification of standard [3], the variation of the PM loop bandwidth should be kept less than ±10%. Considering this variation, the PM loop bandwidth needs calibration. Additionally, it is necessary to calibrate in every burst because of the frequency hop. Therefore, the calibration period should be as short as possible.

Figure 19.7.2 shows the calibration system design. The calibration method for the PM loop can achieve the short calibration period (a few microseconds), and less than ±10% variation of the loop bandwidth after the calibration. The PM loop bandwidth calibration system uses a ΔΣ modulator for the local divider to generate a step signal. The step signal is applied as an input to a phase detector, which is actually the same circuit used by the mixer. The response is detected by a 10b counter and a10b accumulator at the VCO output. The reason to use the ΔΣ modulator is that it makes to the generatation of smaller step signal, such as a 1/8 divide step, possible. The small step can keep the PM loop in the locked state. The output of the devide-by-13 local divider does not have a 50% duty cycle. Therefore, a divide-by-2 is necessary at the output of the divide-by-13 block to maintain a 50% duty cycle. To decrease the ΔΣ noise, a low-pass filter with a cut-off frequency around 60MHz is necessary after the divide-by-2 block.

The PM loop bandwidth calibration procedure is as follows. The ΔΣ modulator first sets the local divider to "13–1/16" during the locked state of the local synthesizer. The signal is applied to the phase detector via the divide-by-2 block and LPF. The downconverted VCO output signal is similarly applied to the phase detector via the divide-by-2 and LPF. When the local signal via the "13–1/16" divider and the downconverted VCO signal are synchronized, the 10b counter and the 10b accumulator at the VCO output are operated for 60 times accumulation (about 1.5μsec) by IF/2 sampling. After the accumulation, the data is kept in a register as "ACC1". Next, the divide ratio is stepped from "13–1/16" to "13+1/16". Triggered by the step, the 10b counter and 10b accumulator are started after being reset. After the accumulation, the accumulated value is kept in a register as "ACC2". Finally, "ACC2–ACC1" is calculated. Because "ACC2–ACC1" is approximately linear with 1/loop-gain, as shown in Fig. 19.7.3 (a), the calibration system can detect the difference between suitable and unsuitable loop gains. Figure 19.7.3 (b) shows the calibrated result. This enables the PM loop to achieve the suitable bandwidth.

In the case of GPRS, the shift between 8PSK and GMSK happens in the adjacent transmitting slot. In this case, the I and Q signals can go through zero. When that happens, the PA output amplitude becomes zero, and the PM and AM loops in the polar loop cannot stay in the locked state. To avoid this phenomenon, a special modulator as shown in Fig. 19.7.4 controls the switching timing between the 8PSK and GMSK filters. The proposed 8PSK and GMSK filters are designed with a 5-symbol tap length. When the data in the digital filter becomes all zero, in terms of constellation diagrams, the I and Q signals draw a 3π/8 phase-shift circle in the case of the EDGE filter and a π/2 phase-shift circle in the case of the GSM filter. This tracking of circles between 8PSK and GMSK is used. When the I/Q points between 8PSK and GMSK become nearest to each other, the RFIC shifts from 8PSK to GMSK or from GMSK to 8PSK. Due to this switching timing, the zero crossing can be avoided as shown in Fig. 19.7.5 (a) and (b).

Figure 19.7.6 shows PA output spectrum masks for both the GSM and EDGE modes. The developed RFIC achieves less than –65dBc at the 400kHz offset in GSM mode and less than –163dBm at the 20MHz offset at the PA output. The rms of modulation phase error is less than 1.9°. In the case of EDGE, less than –59dBc at the 400kHz offset, –65dBc at the 600kHz offset, and 3.1% EVM_{rms} are achieved at the PA output. The results have enough margins for the standard [3]. The developed RFIC draws 60mA in receiving mode, 100mA in GSM mode, and 130mA in EDGE mode from a 2.7V supply.

Acknowledgments:
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References:
[1] Pierre-Henri Bonnaud, Markus Hammes, Andre Hanke, et al., "A Fully Integrated SoC for GSM/GPRS in 0.13μm CMOS," *ISSCC Dig. Tech. Papers,* pp. 482-483, Feb., 2006.
[2] V. PETROVIC and W. Gosling "Polar-loop transmitter," *IEEE Electronics Letters*, Vol.15, No.10, pp. 286-289, May, 1979.
[3] 3GPP TS 05.05 V8.9.0, "Digital Cellular Telecommunications System (Phase 2+); Radio Transmission and Reception."

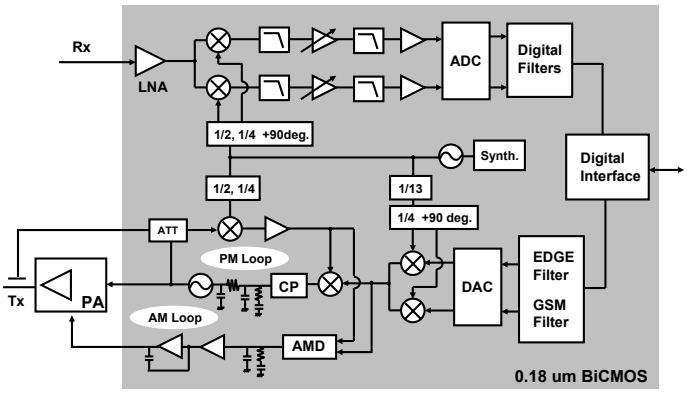

Figure 19.7.1: Block diagram of the polar loop transmitter and the direct-conversion receiver.

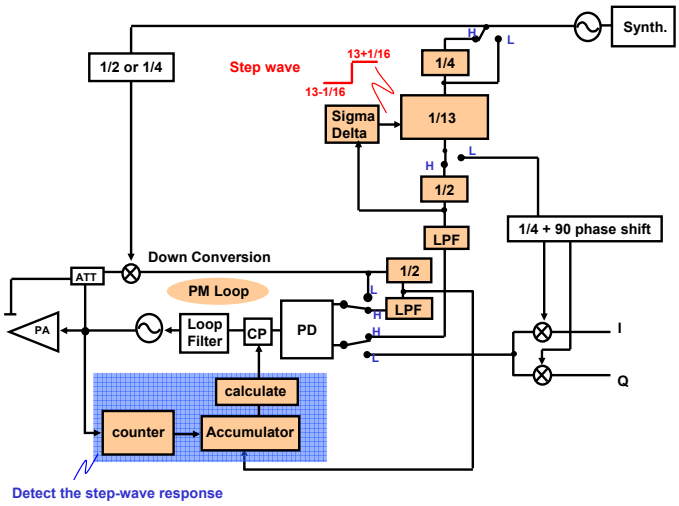

Figure 19.7.2: Block diagram of the PM loop bandwidth calibration.

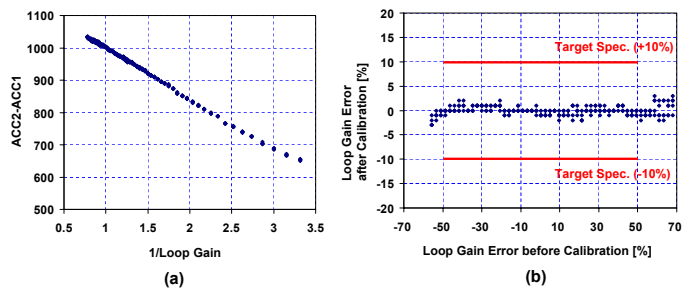

Figure 19.7.3: Evaluation results of PM loop bandwidth calibration.

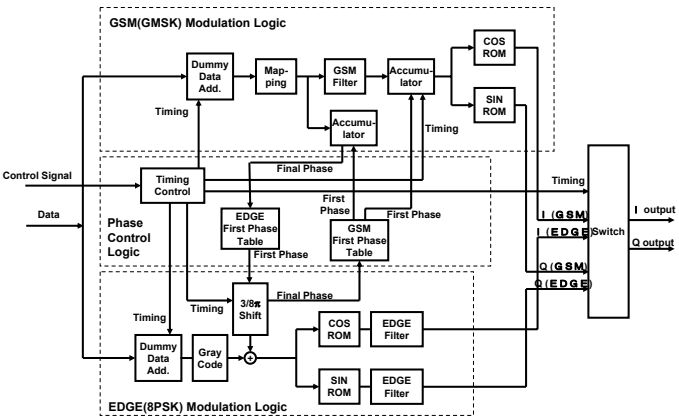

Figure 19.7.4: Block diagram of GMSK and 8PSK filters.

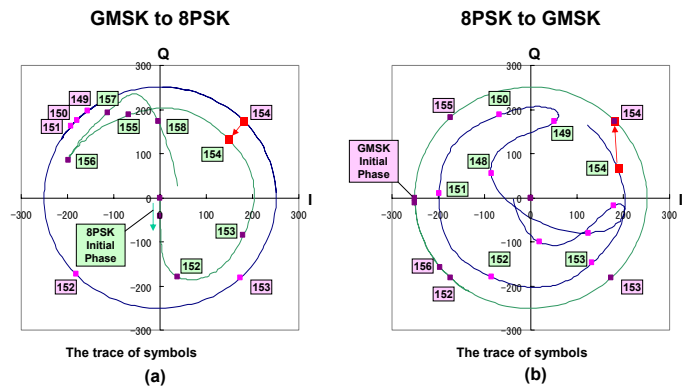

Figure 19.7.5: 8PSK to GMSK transition.

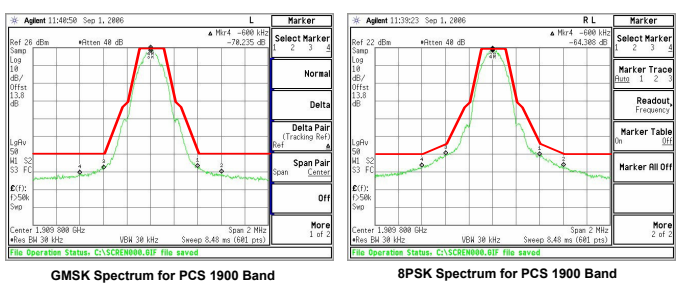

Figure 19.7.6: Spectra of the polar loop transmitter.

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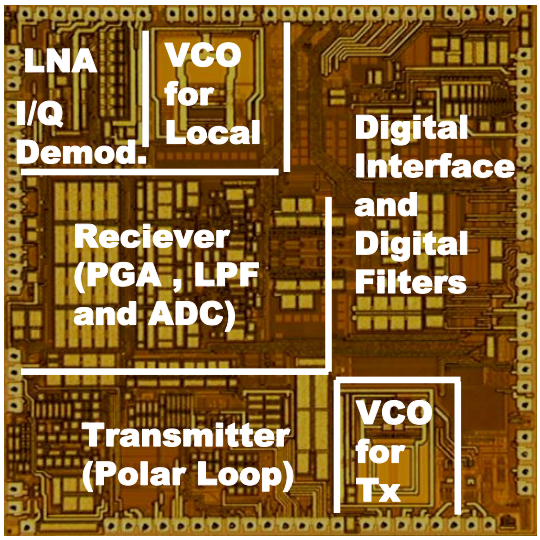

Figure 19.7.7: Die micrograph.

